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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,984	09/07/2000	Anthony M. Chiu	00-C-016	2247

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 08/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/656,984	Applicant(s) CHIU, ANTHONY M.	
	Examiner Khiem D Nguyen	Art Unit 2823	

-- Th MAILING DATE of this communication app ars on the cov r she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04-15-2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,21-25 and 29-31* is/are rejected.

7)☒ Claim(s) *26-28 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the new ground(s) of rejection.

New Grounds of Rejection

Specification

Claim 1 is objected to because of the following informalities: In Claim 1 line 6, delete "unecapsulated" and insert "unencapsulated". Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (USPN. 6,307,258 B1) hereinafter Crane in view of Ichikawa et al. (USPN. 6,165,818) herein after Ichikawa.

With respect to claim 1, Crane show a method of providing electrostatic discharge protection (Figs. 1-2 #100 col. 3 line 62) for an integrated circuit (Figs. 1-2 #10 col. 3 line 57), comprising:

mounting an integrated circuit die (Figs 1-2 # 10 col. 3 line 62) on a lead frame (Figs. 1-2 # 200 col. 3 line 62); encapsulating (col. 4 line 36-40) at least part of the integrated circuit die with a plastic or epoxy material (See col. 4 lines 5-8); and show

folding an unencapsulated portion of the lead frame around sides of the encapsulated integrated circuit die (# 100) but fails to show folding an un-encapsulated portion of lead frame over or adjacent to a peripheral upper surface of the plastic or epoxy material as required in the present claim. However, ***it would have been obvious to one of ordinary skill in the art*** to show folding an un-encapsulated portion of the lead frame over or adjacent to a peripheral upper surface of the plastic or epoxy material as required in the present claim, because selection of any order of performing process steps is prima facie obvious in the absence of new of unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

With respect to claim 2, Crane shows the steps of connecting the portion of the lead frame (Figs. 1 and 2. # 200 col. 3 line 61) around sides of the encapsulated integrated circuit die (Fig. 1 # 100 Col. 3 line 62) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (See col. 4 lines 5-8) but fails to show connection to a ground voltage.

Ichikawa shows a pair of radiating terminals (Figs 1-2 # 2 col. 1 line 64) of the lead frame (Figs. 1-2 # 12 col. 2 line 8) are connected to grounding lines of the circuit board (See col. 1 lines 59-65).

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to show the method of Ichikawa in the process of Crane for connecting some terminals of the lead frame to a ground voltage because in doing so various signals can be inputted to and outputted from the pallet and extra heat is radiated from ground terminals. (See Ichikawa col. 1 lines 66-67 and col. 2 lines 1-2).

With respect to claim 3, Crane show the steps of encapsulating at least part of the integrated circuit die (# 100) with a plastic or epoxy material further comprising: After mounting the integrated circuit die (# 100) on the lead frame (# 200), encapsulating exposed surfaces of the integrated circuit die except for a sensing surface (See Crane col. 4 lines 25-27); and encapsulating wire bonds (Crane Col. 4 lines 12) connecting the integrated circuit die (# 100) through leads (# 300) to portions of the lead frame (# 200). (See crane Figs. 1-2 col. 4 lines 11-18 and col. 4 lines 25-30).

With respect to claim 4, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4). (See Ichikawa col. 1 lines 50-58), folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs.1-2 and Figs. 3-7).

With respect to claim 5, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa, Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame

(Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminal # 33 and 48 of terminal # 32 col. 6 lines 52-65) of the lead frame (Figs. 5 and 6 # 41) around a first side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), wherein the first portion includes an opening (# 37 col. 7 line 43) providing access for a connector (# 44 col. 7 line 47) to pins (Fig. 5 # 45 col. 7 line 48) electrically connected to the integrated circuit die (Figs. 5 and 6 # 31 col. 7 lines 21-26).

folding a first portion (Ichikawa Figs 5 and 6 # 35 and # 36 col. 7 line 41 of terminal # 32 and # 33 col. 7 lines 42-43) of the lead frame (Figs. 5 and 6 # 41) around a first side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), wherein the first portion includes an opening (# 37 col. 7 line 43) providing access for a connector (# 44 col. 7 line 47) to pins (Fig. 5 # 45 col. 7 line 48) electrically connected to the integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 39).

With respect to claim 6, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (#4), and Ichikawa further teach the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame

(Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54 of Ichikawa Figs. 1-2 and Figs. 3-7).

folding a portion (Ichikawa Figs 4-6 terminals # 35 and # 36 col. 7 lines 40-45) of the lead frame (Figs. 5 and 6 # 41) around edges of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40), not including leads (# 32 and # 33) electrically connected to the integrated circuit die (# 31).

With respect to claim 7, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 col. 1 line 52) and over or adjacent to peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminals # 33 and 48 of terminals # 32 col. 6 lines 52-65) of the lead frame (Figs. 5 and 6 # 41) around a side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40); and folding a second portion (# 35 and # 36 of terminal # 32) of the lead frame (# 41) extending from the first portion over a peripheral upper surface of the encapsulated integrated circuit die (# 31). (See col. 7 lines 41-45).

With respect to claim 8, Crane in view of Ichikawa show the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 Col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teach the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around each side (Fig. 4 col. 6 lines 52-54) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). (See Ichikawa Figs. 1-2 and Figs. 3-7).

folding a first portion (Ichikawa Figs. 4-6 # 47 of terminal # 33 and 48 of terminal # 32 col. 6 lines 52-64) of the lead frame (Figs. 5 and 6 # 41) around a side of the encapsulated integrated circuit die (Figs. 5 and 6 # 31 col. 7 line 40); and folding a second portion (# 35 and # 36 of terminal # 32) of the lead frame (# 41) extending from the first portion adjacent to and level with a peripheral upper surface of the encapsulated integrated circuit die (# 31). (See col. 6 lines 66-67 and col. 7 lines 1-4).

3. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (U.S. Patent 6,307,258) in view of Ichikawa et al. (U.S. Patent 6,165,818).

Crane teaches a method of providing electrostatic discharge protection for an integrated circuit, comprising (See Col. 3, line 56 to col. 5, line 30 and FIGS. 1).

mounting the integrated circuit die 100 on a flat lead frame 200, 300 having the lead portions projecting at least one edge and the electrostatic discharge protection portion projecting from at least one edge wherein the electrostatic discharge protection

portion of the lead frame projects from an edge other than an edge from which the lead portions project;

encapsulating at least part of an integrated circuit die 100 mounted on a lead frame 200, 300 and a portion of the lead frame with a plastic or epoxy material, leaving lead portions and an electrostatic discharge protection portion of the lead frame un-encapsulated and further comprising forming the plastic or epoxy material over one surface and sidewalls of the integrated circuit die and over portions of a surface of the lead frame on which the integrated circuit die is mounted, leaving an opposite surface of the lead frame and the lead portions and the electrostatic discharge protection portion of the lead frame unencapsulated and further leaving a contact surface of the integrated circuit die exposed;

folding the electrostatic discharge protection portion of the lead frame around the encapsulated integrated circuit die.

Crane fails to teach folding the electrostatic discharge protection portion of the lead frame over or adjacent to a surface of the plastic or epoxy material as recited in present claim 21.

Ichikawa teaches the steps of folding a portion (Ichikawa outer portions Fig. 3 # 5 and # 6 of terminals # 2 and # 3 col. 1 line 56) of the lead frame (Ichikawa Fig. 3 # 11 col. 2 line 7) around sides of the encapsulated integrated circuit die (Ichikawa Fig. 1 # 4 Col. 1 line 52) and over or adjacent to a peripheral upper surface of the plastic or epoxy material (# 4), and Ichikawa further teaches the steps of folding portions (Ichikawa Fig. 4 # 32, # 33 col. 6 line 58) of the lead frame (Ichikawa Fig. 4 # 41 col. 6 line 47) around

each side (Fig. 4 col. 6 lines 52-61) of the encapsulated integrated circuit die (Ichikawa Fig. 4 # 31 col. 6 line 48). ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Ichikawa teaching into Crane's method because in doing so a semiconductor device which is high in productivity and a lead frame which contributes to improvement in productivity of a semiconductor device can be obtained. See col. 3, lines 8-11.

4. Claims 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Crane, Jr. et al. (U.S. Patent 6,307,258) in view of Ichikawa et al. (U.S. Patent 6,165,818).

Crane teaches a method of providing electrostatic discharge protection for an integrated circuit, comprising (See Col. 3, line 56 to col. 5, line 30 and FIGS. 1).

forming a flat lead frame 200 having lead portions 300 and an electrostatic discharge protection portion extending from edges thereof;

mounting the integrated circuit die 100 on the surface of the lead frame and encapsulating the at least sides of the integrated circuit die and a portion of the lead frame surface on which the integrated circuit die is mounted with an encapsulating material;

folding the electrostatic discharge protection portion of the lead frame around one or more sides of the encapsulating material and further comprising,

folding the electrostatic discharge protection portion of the lead frame to extend along the sides of the encapsulating material;

folding the electrostatic discharge protection portion of the lead frame to extend over a periphery of a surface or adjacent to a surface of the encapsulating material opposite the lead frame; and

folding the electrostatic discharge protection portion of the lead frame around at least two opposing sides of the encapsulating material.

Crane fails to teach leaving the lead portions and the electrostatic discharge protection portion of the lead frame projecting beyond and extending adjacent to a surface of the encapsulating opposite the lead frame the encapsulating material as recited in present claims 29 and 31.

Ichikawa teaches mounting an integrated circuit device 31 on a surface of the lead frame 41 having plurality of lead terminals 33 formed projecting beyond the encapsulating material 34 and the plurality of lead terminals are arranged at positions adjacent to the radiating terminals 32. See col. 6, lines 10-29 and FIGS. 4-7. ***It would have been obvious to one of ordinary skill in the art of making semiconductor devices*** to incorporate Ichikawa teaching into Crane's method because in doing so a semiconductor device which high in productivity and a lead frame which contributes to improvement in productivity of a semiconductor device can be obtained. See col. 3, lines 8-11.

Allowable Subject Matter

5. Claims 26-28 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
August 3, 2002

LONG PHAM
PRIMARY EXAMINER